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by *Gupta, Uma G.*

IEEE Computer Society Press, c1991.

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3. Immune and receptor assays in theory and practice / Patrick Englebienne.

by *Englebienne, Patrick.*

CRC Press, c2000.

Call No.: QP519.9.I42 E54 2000

4. Credit risk modeling : design and application / Elizabeth Mays, editor.

by *Mays, Elizabeth (Freda Elizabeth)*

Glenlake Pub. Co. ; AMACOM c1998.

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5. Clinical data management / edited by Richard Rondel, Sheila Varley, Colin Webb.

by *Rondel, R. K.*

Wiley, c2000.

Call No.: R853.D37 C55 2000

6. Integrated formal methods : second international conference, IFM 2000, Dagstuhl Castle, Germany, November 1-3, 2000 : proceedings / Wolfgang Grieskamp, Thomas Santen, Bill Stoddart (eds.).

by *International Conference on Integrated Formal Methods (2nd : 2000 : Dagstuhl Castle, Germany)*
Springer, 2000.

Call No.: QA76.9.F67 I58 2000

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7. Neural networks and artificial intelligence for biomedical engineering / Donna L. Hudson, Maurice E. Cohen.

by *Hudson, D. L. (Donna L.)*
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12. Software engineering metrics / edited by Martin Shepperd.

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14. Tutorial, software testing & validation techniques / [compiled by] Edward Miller, William E. Howden.

by *Miller, Edward, 1941-*

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15. Derivation and validation of software metrics / Martin Shepperd and Darrel Ince.

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Clarendon Press ; Oxford University Press, 1993.

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by *Berry, Ira R., 1942-*

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20. A first look at ASP.NET v. 2.0 [electronic resource]/ Alex Homer, Dave Sussman, Rob Howard.

by *Homer, Alex.*

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by *Freeman, Adam.*
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23. Manufacturing of gene therapeutics [electronic resource] : methods, processing, regulation, and validation / edited by G. Subramanian.

by *Subramanian, G., 1935-*
Kluwer Academic/Plenum Publishers, c2002.
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24. Validation of pharmaceutical processes [electronic resource] : sterile products / edited by Frederick J. Carleton, James P. Agalloco.

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Process validation for manufacturing of biologics and biotechnology products : Berlin Hilton Hotel, Berlin, Germany, 6 - 7 September, 2001 / volume editors, Fred Brown, Anthony S. Lubiniecki.

by *Brown, Fred*, 1925-
Karger, c2003.

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28. Validation of critical signals for the safety parameter display system / prepared by Babcock & Wilcox Company ; principal investigators, B.J. Benedict, R.I. Lutz, L.P. Smith ; subcontractor, the Charles Stark Draper Laboratory Inc. ; principal investigator, O.L. Deutsch ; prepared for Electric Power Research Institute.

by *Benedict, B. J.*
The Institute, [1987]

Call No.: TK1078 .B46 1987

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29. Telescope structures, enclosures, controls, assembly/integration/validation, and commissioning : 27-31 March 2000, Munich, Germany / Thomas A. Sebring, Torben Andersen, chairs/editors ; sponsored by SPIE--the International Society for Optical Engineering ; cosponsored by the European Southern Observatory ; corporate sponsor DFM Engineering, Inc.

by *Sebring, Thomas A.*
SPIE, 2000.

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30. Analytical method development and validation [electronic resource] / Michael Swartz, Ira S. Krull.

by *Swartz, Michael (Michael E.)*
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by *Rajsuman, Rochit.*

Artech House, 2000.

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Verification by error modeling : using testing techniques in hardware verification /

Author: Radecka, Katarzyna.
Zilic, Zeljko.

Imprint: Boston : Kluwer Academic Publishers, 2003.

Notes: Includes bibliographical references and index.

ISBN: 1402076525 (alk. paper)

Subjects: Integrated circuits -- Very large scale integration -- Computer-aided design.

Integrated circuits -- Verification.
Error analysis (Mathematics)

Series: Frontiers in electronic testing ;

Description: xiv, 216 p. : ill. ; 25 cm.

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Author: CHARME'99 (1999 : Bad Herrenalb, Germany)
Pierre, Laurence.
Kropf, Thomas, 1961-

Imprint: Berlin : New York : Springer, 1999.

URL: <http://link.springer-ny.com/link/service/series/0558/tocs/t1703.htm> Click here to see page images available via Springer.

ISBN: 3540665595 (pbk.)

Subjects: Integrated circuits -- Very large scale integration -- Computer-aided design -- Congresses.
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by *Advanced Research Workshop on Correct Hardware Design Methodologies*.

Springer, 1984-

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2. Model checking / Edmund M. Clarke, Jr., Orna Grumberg, and Doron A. Peled.

by *Clarke, E. M., 1945-*

MIT Press, c1999.

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3. Tools and algorithms for the construction and analysis of systems : 7th international conference, TACAS 2001 : proceedings / Tiziana Margaria, Wang Yi (eds.).

by *TACAS 2001 (2001 : Genoa, Italy)*

Springer, c2001.

Call No.: QA76.9.S88 T33 2001

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4. Principles of verifiable RTL design : a functional coding style supporting verification processes in Verilog / Lionel Bening and Harry Foster.

by *Bening, Lionel, 1939-*

Kluwer Academic Publishers, c2001.

Call No.: TK7874.75 .B47 2001

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5. Correct hardware design and verification methods [electronic resource] : 10th IFIP WG10.5 advanced research working conference, CHARME'99, Bad Herrenalb, Germany,

September 27-29, 1999 : proceedings / Laurence Pierre, Thomas Kropf (eds.).

by *CHARME'99 (1999 : Bad Herrenalb, Germany)*

Springer, 1999.

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- 6. Correct hardware design and verification methods [electronic resource] : 11th IFIP WG 10.5 Advanced Research Working Conference, CHARME 2001, Livingston, Scotland, UK, September 4-7, 2001 : proceedings / Tiziana Margaria, Tom Melham (eds.)**

by *CHARME 2001 (2001 : Livingston, Scotland)*

Springer, c2001.

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- 7. Verification by error modeling : using testing techniques in hardware verification / written by Katarzyna Radecka, Zeljko Zilic.**

by *Radecka, Katarzyna.*

Kluwer Academic Publishers, 2003.

Call No.: TK7874.75 .R33 2003

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- 8. Design verification with e [electronic resource]/ Samir Palnitkar.**

by *Palnitkar, Samir.*

Prentice Hall PTR, 2004.

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S2	43	(BERTSCH-JOHN-E BERTSCH-JOHN-EDWARD BERTSCH-JOHN COOPS-DANIEL-S FRIED-DAVID FRIED-DAVID-M).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/09/30 12:08
S3	1	(model same hardware same correlation) and MHC	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 10:29
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S7	659	wafer with final with test	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 10:52
S8	223	(wafer with final with test) and (line with test)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 10:57
S9	91	(wafer with final with test) and (in with line with test)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 10:57
S10	1	(model same hardware same correlation) and ((wafer with final with test) and (in with line with test))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 11:22
S11	1581	(mos or cmos or mosfet) same (verify or verification or verifying)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 11:23
S12	248	((mos or cmos or mosfet) same (verify or verification or verifying)) and wafer	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 11:24

S13	8	((((mos or cmos or mosfet) same (verify or verification or verifying)) and wafer) and (source adj current) and (drain adj current))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 11:40
S14	89	((((mos or cmos or mosfet) same (verify or verification or verifying)) and wafer) and (source with current) and (drain with current))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/01 11:26
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S19	151	spice and wafer and model and (test or verif\$7) and parameter	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/12 13:44
S20	5	spice and wafer and model and (test or verif\$7) and parameter and "702"/\$3.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/06 17:07
S21	185	spice and (wafer and model) and (test or verif\$7)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/12 13:45
S22	39	spice and ((wafer and model) same (test or verif\$7))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/12 13:45
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S24	23	kerf same oscillator	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:43

S25	1079	700/121.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:43
S26	218	700/121.ccls. and (delay or hysteresis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:51
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S33	95	700/108.ccls. and (delay or hysteresis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:57
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S36	34	((700/108.ccls. and (delay or hysteresis)) or (700/108.ccls. and (delay or hysteresis))) and wafer	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:52

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S42	13	((700/109.ccls. and (delay or hysteresis or hysteresis)) and wafer) and (model\$5 or simulat\$5 or emulat\$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:58
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S44	50	700/110.ccls. and (delay or hysteresis or hysteresis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:58
S45	19	(700/110.ccls. and (delay or hysteresis or hysteresis)) and wafer	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:58
S46	11	((700/110.ccls. and (delay or hysteresis or hysteresis)) and wafer) and (model\$5 or simulat\$5 or emulat\$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:58
S47	2	((((700/110.ccls. and (delay or hysteresis or hysteresis)) and wafer) and (model\$5 or simulat\$5 or emulat\$5)) and (threshold with voltage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/10/13 22:58

S48	8	model adj hardware adj correlat\$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/15 15:46
S49	18	(design adj (valid\$6 or verif\$7)) and (remov\$4 same defect\$4 same data)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/15 15:48
S50	19	(design adj (valid\$6 or verif\$7)) and ((remov\$4 or delet\$4 or ignor\$4 or disregard\$4) same defect\$4 same data)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/15 18:19
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